IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

Appl. No: 10/552,076

Applicant(s): Andre Terechko

Filed: October 4, 2005

TC/A.U.: 2100/2196

Examiner: Keith Vicary

Atty. Docket: NL 030344

Title: DATA PROCESSING SYSTEM WITH CLUSTERED ILP PROCESSOR

APPEAL BRIEF

Honorable Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In connection with the Notice of Appeal dated July 6, 2007, Applicants provide the following Appeal Brief in the above captioned application.

TABLE OF CASES

1. Real Party in Interest

The real party in interest as assignee of the entire right and title to the invention described in the present application is Koninklijke Philips N.V. having a principle place of business at Groenewoudseweg 2, Eindhoven, The Netherlands.

2. Related Appeals and Interferences

There are no known related appeals or interferences at this time.

3. Status of the Claims

Claims 1-8 are pending in the present application. All have been finally rejected. The rejected claims 1-8 are duplicated in the Appendix.

4. Status of Amendments

A final Office Action on the merits was mailed on April 6, 2007. A Response to the Final Office Action was filed on June 6, 2007, traversing the rejections of the final Office Action. A Notice of Appeal was filed on July 6, 2007.

5. Summary of the Claimed Subject Matter[1]

In a representative embodiment, a data processing system comprises a clustered Instruction Level Parallelism processor, comprising a plurality of clusters (A, B, C, D) each comprising at least one register file and at least one functional unit. The system also comprises an instruction unit (e.g., IFD) for issuing control signals to the clusters (A-D). The instruction unit is connected to each of the clusters via respective control connections (CA, CB,CC, CD), and one or more additional pipeline registers (P) is arranged in the control connections depending on the distance between the instruction unit (IFD) and the clusters (A-D). The pipeline registers (P) are adapted to provide a dedicated direct signal data signal connection (shown as solid lines in Fig. 1) between any two of the clusters. (Kindly refer to Figs. 1, page 4, line 18-line 29, and claim 1.)

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1 In the description to follow, citations to variouslaims, reference numerals, drawings and corresponding text in the specification are provided solely to comply with Patent Office RulesIt is emphasized that these reference numerals, drawings and text are representative in nature, and in not any way limiting of the true scope ofite claims. It would therefore be improper to import any meaning into any of the claims simply on the basis of illustrative language that is provided here only under obligation to satisfy Patent Office rules for

In accordance with another representative embodiment, a clustered Instruction Level Parallelism processor comprises a plurality of clusters (A, B, C, D), each comprising at least one register file and at least one functional unit. The processor also comprises an instruction unit (e.g., IFD) for issuing control signals to the clusters (A-D). The instruction unit is connected to each of the clusters via respective control connections (CA, CB,CC, CD), and one or more additional pipeline registers (P) is arranged in the control connections depending on the distance between the instruction unit (IFD) and the clusters (A-D). The pipeline registers (P) are adapted to provide a dedicated direct signal data signal connection (shown as solid lines in Fig. 1) between any two of the clusters. (Kindly refer to Figs. 1, page 4, line 18-line 29, and claim 5.)

6. Grounds of Rejection to be Reviewed on Appeal

The issues in the present matter are whether:

I. The title of the invention is properly objected;

II. Claims 1-8 are properly rejected under 35 U.S.C. § 112, Second Paragraph as being indefinite for failing to particularly point out and distinctly claim the invention;

III. Claims 1-3 and 5-7 are properly rejected under 35 U.S.C. § 103(a) in view of *Batten, et al.* (U.S. Patent 6,269,437), further in view of *Nickolls, et al.* (U.S. Patent 5,598,408); and

IV. Claims 4 and 8 are properly rejected under 35 U.S.C. § 103(a) in view of *Batten, et al.* further in view of *Nichols, et al.* and further in view of *Pechanek, et al.* (U.S. Patent 5,659,785).

7. Argument

Applicants respectfully traverse all objections and rejections for at least the reasons set forth herein.

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maintaining an Appeal.

I. Objection to the Title

The Title is objected to as being non-descriptive. As stated in the Response under Rule 116, the Office Action alleges that the title "DATA PROCESSING SYSTEM WITH CLUSTERED ILP PROCESSOR" is non-descriptive and thus not indicative of the claimed subject matter. At the outset, there is no basis in law provided, or any standard thereof provided in support of this objection. Accordingly, Applicants respectfully submit that this objection is without merit and must be withdrawn.

The above notwithstanding, Applicants note, for example, that claim 1 is drawn to a data processing system and features:

"...*a clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;...*"

Applicants thus submit that the title is highly descriptive of the claimed subject matter of at least claim 1.

For at least the reasons set forth above, Applicants respectfully submit that the objection to the title/specification is improper and should be withdrawn.

II. Rejection of claims 1-8 under 35 U.S.C. § 112, Second Paragraph as being indefinite for failing to particularly point out and distinctly claim the invention

Claims 1-8 are rejected under section 112 of the Code for alleged indefiniteness. Applicants respectfully disagree, and note that the application as filed clear discloses the questioned relationship.

The Examiner asserts:

b. In claim 1, lines 9-10 and claim 5, lines 9-10, the applicant's amended claims disclose "said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters." It is indefinite as to how a pipeline register may solely provide a connection between any two of said clusters, as opposed to the connection between the instruction unit and the clusters, which is connected by both a pipeline register and respective control connections. Furthermore, it is indefinite as to if the same pipeline registers are being used as part of both the control connections and the data connections, or whether a subset of the pipeline registers are being used for one type of connection, and the remaining pipeline registers for the other type of connection.

A connection of cluster according to an embodiment described in the filed application is described:

"In Fig. 1 a clustered VLIW architecture with a full point-to-point connectivity topology according to a first embodiment is shown. The architecture includes four clusters, namely clusters **A, B, C and D, which are fully connected to each other and an instruction fetch/dispatch unit IFD being connected to each cluster A-D via control connections paths CA-CD.** Accordingly, **there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.** The latency of an inter-cluster transfer of data is always the same for every inter-cluster connection independent of the actual distance between the clusters on the chip. The actual distance on the chip between the clusters A and C, and clusters B and D is considered to be longer than the distance between the clusters A and D, A and B, B and C, as well as C and D. Therefore, a pipeline register P is arranged in the control connection paths CC and CD,

in order to pipeline the control signals to remote clusters C, D."

(Emphasis Provided).

From the description in the filed application in which the signal connection featured in claim 1 is provided verbatim, one can garner how the dedicated signal connection is realized.

Accordingly, and for at least the reasons set forth in above, Applicants respectfully submit that the dedicated direct signal connection between any two clusters is well within the requirements of 35 U.S.C. § 112, ¶ 2. Therefore, Applicants respectfully traverse this rejection as being improper.

III. Rejection of claims 1-3 and 5-7 under 35 U.S.C. § 103(a)

Claims 1-3 and 5-7 are rejected under 35 U.S.C. § 103(a) in view of *Batten, et al.* (U.S. Patent 6,269,437), further in view of *Nickolls, et al.* (U.S. Patent 5,598,408). For at least the reason set forth herein, Applicants respectfully submit that this rejection is improper and should be withdrawn.

At the outset, Applicants rely at least on the following standard of law as it relates to obviousness. Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. While the sequence of these questions might be reordered in any particular case, the factors continue to define the inquiry that controls. If a court, or patent examiner, conducts this analysis and concludes the claimed subject matter was obvious, the claim is invalid under § 103. *KSR Int'l Co. v. Teleflex Inc.,* 127 S. Ct. 1727; 82 U.S.P.Q.2D 1385 (2007), citing, in part *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966).

The Court in *KSR* continued: "A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex*

post reasoning. See *Graham*, 383 U.S., at 36, 86 S. Ct. 684, 15 L. Ed. 2d 545 (warning against a "temptation to read into the prior art the teachings of the invention in issue" and instructing courts to "'guard against slipping into the use of hindsight'" (quoting *Monroe Auto Equipment Co.* v. *Heckethorn Mfg. & Supply Co.*, 332 F.2d 406, 412 (CA6 1964))).

Claims 1 and 5, as amended, include pipeline registers *adapted to provide a dedicated direct signal data signal connection between any two of the clusters.*

In Fig. 1 of the filed application, a clustered VLIW architecture with a full point-to-point connectivity topology according to a first embodiment is shown. The architecture includes four clusters, namely clusters A, B, C and D, which are fully connected to each other and an instruction fetch/dispatch unit IFD connected to each cluster A-D via control connections paths CA-CD. Accordingly, there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.

The Office Action directs Applicants to column 10, lines 25-26 and lines 31-35 in asserting that the noted feature of claim 1 is taught by *Batten, et al.* Applicants respectfully disagree.

The reference to *Batten, et al.* discloses in the Abstract that:

"[T]he processor includes multiple clusters of execution units, with each of the clusters having a portion of a register file and a portion of a predicate file associated therewith, such that a given cluster is permitted to write to and read from its associated portions of the register and predicate files. A duplicator interconnection technique in accordance with the invention reduces port pressure by providing one or more global move units in the processor. A given global move unit uses an inter-cluster move instruction to copy a value from a portion of the register or predicate file associated with a source cluster to another portion of the register or predicate file associated with a destination cluster."

A review, for example of Fig.12 of the filed application reveals no dedicated connection between clusters. Moreover, the cited portion of column 10 fails to disclose the dedicated connection between clusters. Finally, the portion of the Office Action

reproduced presently does not present evidence of such as connection. To wit, the Office Action states:

> and said pipeline registers being adapted to provide a dedicated direct signal connection between any two of said clusters (col. 10, lines 25-26 disclose that example O2 was fully connected; col. 10, lines 31-35 validate the meaning of fully connected by saying a topology that is not fully connected comes at the expense of reduced connectivity, requiring additional move instructions; col. 3, line 23-43 go into detail about the arrangement).

At the outset, organizations O1 and O2 include branch units, memory units and a prescribed number of ALUs. The Office Action fails to articulate clearly the disclosure in the reference of connections' between clusters being dedicated as claimed. Finally, a review of column 3, lines 23-43 fails to elucidate the alleged dedicated connection either. Rather the need to specify the degree of access and method of communication between clusters is disclosed; without disclosure of a dedicated connection.

Accordingly, because the applied art fails to disclose at least one feature of independent claim 1 and independent claim 5, a *prima facie* case of obviousness cannot be made based thereon. Thus, claims 1 and 5 are patentable over the applied art. Moreover, claims 2-4 and 6-8, which depend from claims 1 and 5, respectively, are patentable at least for the same reasons as claims 1 and 5. Allowance is earnestly solicited.

Therefore, because the applied art fails to disclose at least one element of claim 1 and of claim 10, a proper prima facie case of obviousness has not been established. Accordingly claim 1 and the claims that depend therefrom, and claim 10 are patentable over the applied art.

Finally, in response to substantially identical arguments and evidence of patentability, the Examiner stated:

14. Applicant's arguments filed 3/15/2007 have been fully considered but they are not persuasive. Therefore the rejection of the original claims is maintained.

15. In the remarks, applicants argued that the prior art of reference do not teach the newly added limitation in independent claims 1 and 5.

16. Examiner respectfully traverses applicant's remarks.

17. As explained above in the rejection of claims, the prior art of record does teach the newly added limitation in independent claims 1 and 5.

Respectfully, Applicants have provided substantial arguments in support of their position. In response, the rejections previously made were maintained and without more, the claims rejected and arguments in support of patentability dismissed out of hand. Applicants respectfully submit that this is improper for not providing support for why the Applicants' position is not persuasive, and not in accordance with MPEP § 706.

8. Conclusion

In view of the foregoing, applicant(s) respectfully request(s): the withdrawal of all objections and rejections of record; the allowance of all the pending claims; and the holding of the application in condition for allowance.

Respectfully submitted on behalf of:

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Appendix

Claims on Appeal

Claims on Appeal:

1. Data processing system comprising:

- a clustered Instruction Level Parallelism processor, comprising a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections, and

one or more additional pipeline registers is arranged in said control connections depending on the distance between said instruction unit and said clusters, said pipeline registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters.

2. Data processing system according to claim 1, wherein

said clusters are connected to each other via a point-to-point connection.

3. Data processing system according to claim 1, wherein

said clusters are connected to each other via a bus connection.

4. Data processing system according to claim 3, wherein

said control connections are implemented as a bus.

5. A clustered Instruction Level Parallelism processor, comprising:

- a plurality of clusters each comprising at least one register file and at least one functional unit;
- an instruction unit for issuing control signals to said clusters,

wherein said instruction unit is connected to each of said clusters via respective control connections, and

one or more additional pipeline registers are arranged in said control connections depending on the distance between said instruction unit and clusters, said pipeline

registers being adapted to provide a dedicated direct signal data signal connection between any two of said clusters.

6. The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a point-to-point connection.

7. The clustered Instruction Level Parallelism processor as claimed in claim 5, wherein said clusters are connected to each other via a bus connection.

8. The clustered Instruction Level Parallelism processor as claimed in claim 7, wherein said control connections are implemented as a bus.

Appendix

Evidence (None)

Appendix

Related Proceedings (None)